Optimal Low Complex Error Collection Parallel Decoding with Extended Golay Code

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ABSTRACT

In this paper, we present a low complex error collection parallel decoding architecture to speed up the decoding process. It further uses a triple layered mechanism to reduce the errors by determining the error location in each position of the codeword received without computation of the location using an error polynomial. A full parallel low delay non-binary decoder is designed with orthogonal Latin squares in Galois field using Golay codes to improve the speed and simultaneously reducing the error. The system is operated in such a way that it reduces the complexity in allowing the decoding to operate with maximum speed and with lower latency. The performance is evaluated on a 64 and 128-bit codes over the Galois Filed in a 45 nm CMOS process. The proposed architecture outperforms other methods in reducing the latency, capacity, delay and area.

Keywords: *Low Complex, Error Collection, Parallel Decoding, CMOS*

INTRODUCTION

Integrated circuits tend to increase density and boost performance as technology is decreasing. Circuits are more vulnerable to external disturbance [1] with smaller geometries and other parameters such as lower voltage. Sources of radiation causes several undesirable effects in profound submicron technologies that endanger the credibility and efficiency of the circuits. As particles enter the material, they can create free transmitters, which can eventually rotate memory cell contents through propagation processes. This condition is known as a Single Event Disorder (SED), one of the major memory fault tolerance issues [2]. For example, spaces are greater than the sum and intense of radiation sources in harsh environments. This is especially important. This type of bit reverse normally removes the content of the memory and thus alters the data. Mechanisms for detecting errors and correcting them are

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important, particularly for systems operating under harsh conditions.

Safeguard or protection against SEDs is developed by various methods. There is an agreement with both of these approaches between the amount of protection obtained and the overheads. This overhead is because additional bits are required to store user data, and some hardware to encrypt and decode data when entering your storage. One of the easiest approaches to error-saving is a parity mechanism that is relatively lightweight but with relatively reduced safety power (just single error detection). The standard method [3] for error code correction or extended error correction hamming codes and two error detection systems are used to ensure proper functionality.

This level is traditionally appropriate, but in recent times there have been more cell upsets (MCUs) [4]. It is natural when smaller geometries are influenced if a particle strikes memory cells [1]. The conventional methods dealing with MCUs uses mainly the interlocking technique [5]. In the faraway field the bits of the same logical concept are allocated. This includes the incorporation of bits from the separate logical terms in adjacent physical locations. If any of these bits is affected by an MCU each bit tapestry is linked to different logical terms that can be fixed with the above simplest SEC mechanisms. Unfortunately, interlocking is not recommended in every situation, since it increases the power and access time and then complicates memory structure [5]. It may also not be possible with minimal memories or strict performance limits.

MCU stability is not the only problem for memories. If more "static" applications, for example, are not regularly accessed by memory, error build up can lead to the problem. If occurs when a SED accumulates more particle in memory to a certain extent but does not gets fixed by an ECCs(Error Correction Code). Scrubbing machines [6] are periodically used to search fix errors against background accumulation in order to overcome this situation. In addition to a reduction in memory access bandwidth, however, this results in an increase in energy consumption. For this, more powerful ECCs that are capable of fixing several bits are also necessary. ECCs are mainly used in high-speed digital fields to minimise the risk of error. The problem is that these codes also demand higher overheads while providing greater protection. For the sake of good memory protection, it is therefore important to design code to minimise these overheads.

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A broad variety of ECCs are typical in multiple bits, as well as in [7]- [11]. Moreover, multiple codes have recently been suggested in order to reduce the device load and delay and to surrender parity time [12], with a low degree of complexity and the balance between latency and parity. For these codes, the maximum number of patterns to be checked per bit is, which is why bursting is limited to a capacity of 4 bit.

RS codes provide an interesting solution, since they are non-binary, i.e. function in Galois field symbols, identified for example by a number of bit. In short, RS codes will correction symbols and all errors are corrected when multiple errors simultaneously affect a symbol (various bits of the symbol) [14]. OLS codes are mostly used for protect the memory against errors because of their quick decoding. This is because it is an OS-MLD [8] that has a very low latency and the majority of these steps can be decoded. Although OLS codes may be binary, nonbinary versions give the same correction as before.

A Shortened Golay Binary Code is an ECC that helps to correct random errors across 23 digit blocks (SBGC). The SBGC is a shortened BGC version, the ideal code for reducing system complexity. There are some BGC algorithms, but most techniques are impracticable.

This can be done through the multi-classification and improves binary decisions of ECC, such as those provided here, which may be solved by other solutions such as ECOC [15]. However applications with memory systems are inaccessible with these solutions in real-time. Some training samples are needed in order to improve the ability to correct errors, and systems need to have a co-processor that may increase the delay greater than 1 ns. For example, if memory contents have to be retrieved offline without real-time processing using a computer, these solutions may be interesting [13].

To resolve this, the study presents a low complex error collection parallel decoding architecture that helps in speeding up the process of decoding.

The main contribution of the paper is given below:

- The study uses a triple layered mechanism to reduce the errors by determining the error location in each position of the codeword received.
- The study design a full parallel low delay non-binary decoder in Galois field using Golay codes.
- The study improves increases the computational speed with reduced error rate and reduced complexity and lower latency.

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RELATED WORKS

Liu, Y. H., & Poulin, D. (2019) trained back propagation neural decoders with an error-adjusted loss function for low density quantum parity control codes. Education will greatly enhance BP decoder efficiency for all the family of codes we check and solve the degeneration problem, which will harm the deciphering of low quantum density parity check codes [16].

Van Wonterghem et al. (2016) compared the performance of long linear binary codes on the binary erasure channel and binary input Gaussian-channel (2016). The Gaussian erasure decoder can be disabled and any binary block code can be decoded using the Gaussian channel. This decoder has a maximum likelihood for Gaussian removal. In comparative with classical error correction systems, Coşkun, M.C. et al. (2019) have evaluated some of the most promising code constructions for short block structures [17].

Guenda, K., et al. (2018) showed that this number is related to the hull of the classical code. The study constructs Entanglement-assisted quantum error correcting codes (EAQECCs) ensures desirable entanglement. This is how the study establish methods to construct EAQECCs that involve desirable interposition quantities. This allows EAQECC families to be erroneously constructed. We also build LCD codes with complete EAQECC interconnections [19].

Fritzmann, T., et al. (2018) discuss how error tolerance in protocols can be increased through the implementation of error correction codes. We concentrate for our case study on NewHope Simple, which has recently been initiated, with four separate error fixation options being suggested and evaluated. The study demonstrate that the combination of traditional and modern BCH and LDPC codes will benefit from grid cryptography [20].

Brandao, F. G., et al. (2019) formed new relations between quantum error correcting codes and approximate quantum error correction codes [21]. Schibisch, S., et al. (2018) demonstrates that ECC, without losing tool-set recognised transmission symbols, can be used to build the marked data set for fine tuning of training [22].

Woods, M. P., & Alhambra, Á. M. (2020) shows the straight connection between this error's smallness and quantum timepiece accuracy and the no-go theorem is broken if it can be measured in quantum mechanics. The asymptotic scale of the error is analysed in a range of scenarios of reference

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systems and error modelling [23].

Bolt, A., et al. (2016) reveal a broad group of high-meshed cluster countries known as Calderbank-Steane-Shor code for quantum error correction codes. This becomes primitive in a protocol that converts a number of these cluster states into a much broader cluster state, with foliated quantum error correction. This design is demonstrated by many established quantum error codes and a structured decoding method is proposed for foliate codes [24].

Swaminathan, R., & Madhukumar, A. S. (2017) suggested joint recognition algorithms for FEC code type and interleaver parameter with no knowledge of Channel Encoder. The algorithm suggested is a block codified, coded and uncoded classification of incoming Information Symbols. In addition, analysis and histogram methods for defining and estimating the threshold value of code are suggested. The results of the simulation demonstrate that code classification and interleaver parameter estimation are effective under incorrect channel conditions [25].

Niu, M. Y., et al. (2018) establish Quantum Error Correction (QEC) symmetry-operator structure was designed based on simple system-dynamic properties. These QEC codes detect photon losses or photon losses and correct these errors with the Hamiltonian production and linear transformations with the photon numeral parity measurements [26].

PROPOSED METHODOLOGY

In this section, we design a low complex error collection parallel decoding architecture with a triple layered error correction mechanism that helps in reduction of errors associated with decoding computations. Design procedure of parallel decoding using Cadence virtuoso software is shown in Figure 1.

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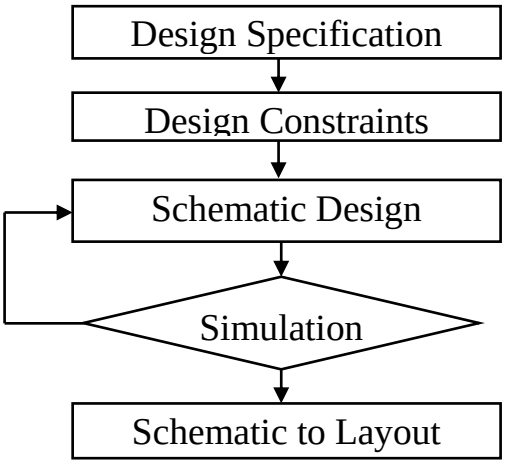

Figure 1. Design Flow

Triple Error Correction decoder

As illustrated in Figure 2, the decoder for BCH with the proposed m-SBS algorithm is SC, DC and EL. The three blocks below are shown in Figure 2.

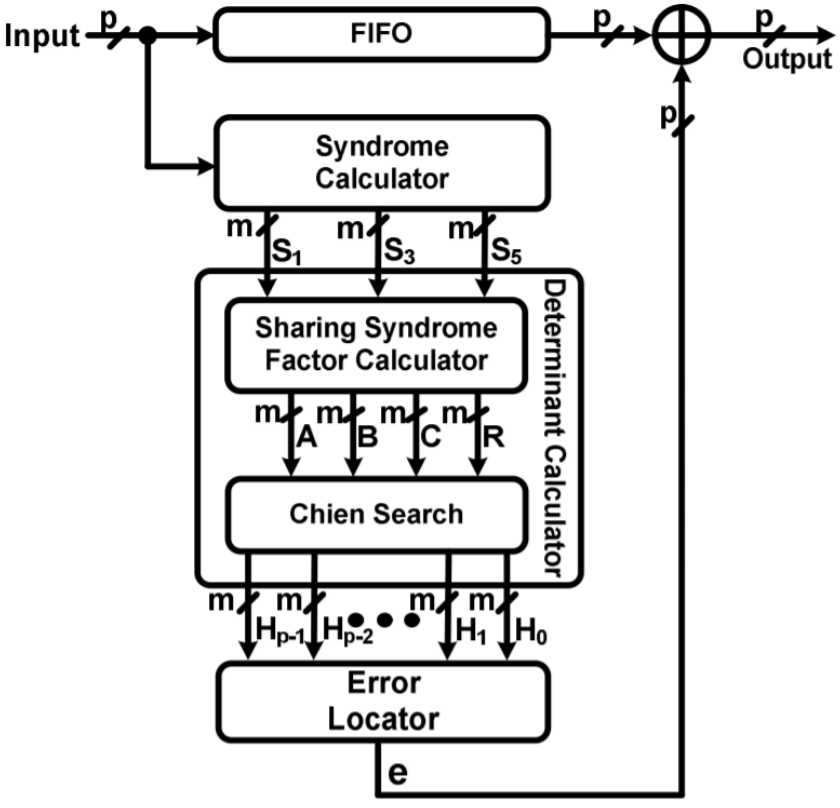

Figure 2. Triple error correction decoder

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***Syndrome Calculator*:** All syndromes of the SC will be determined by adding the roots of the generator in the polynomial $r(x)$. In order to determine the m-SBS triple error correction, BCH algorithms based on S_i are needed as defined [27]. The SC requires a parallel SC cell as seen in the figure when a parallel codeword is obtained in Figure 2.

***Determinant Calculator*:** The DC is used to estimate the determinant value using a syndrome value that checks the error position of the bit. For one bit decoding in the existing decoding has a single DC block and this is considered appropriate, because the DC can only verify one bit in the same clock cycle [28]. A parallel architecture is essential for the measurement of the determining the multi-bit position. The complexity is higher than other blocks which gives a high hardware complexity to the parallel decoder. Thus, it is necessary to reduce the hardware complexity of DC such that it may reduce the decoder complexity.

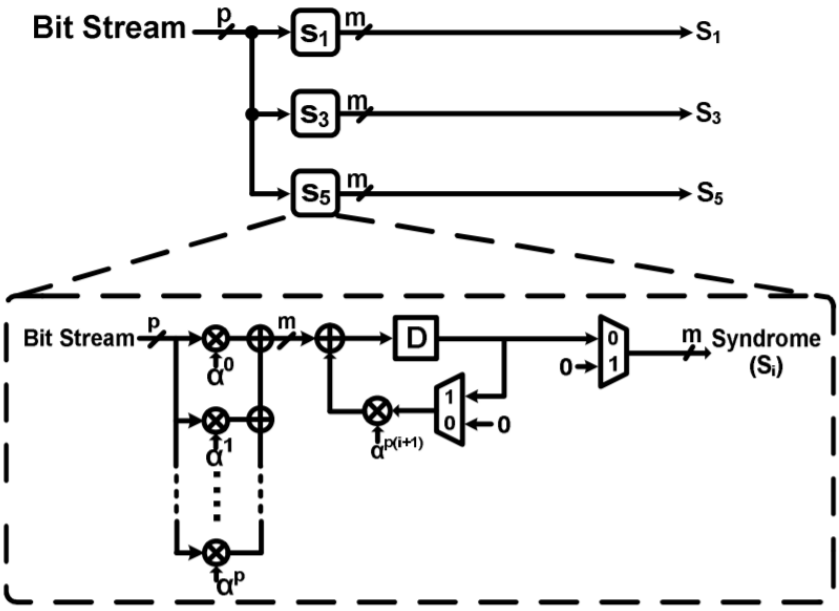

Figure 3. Parallel syndrome calculator in GF(2^{10})

Just two references to the author's best information are available for non-binary OLS. The two contributions classify non-binary OLS as a 2t m/m2 subset (which describes a square in the Latin format m of each submatrix, an MSF matrix with m permutations in their rows and columns) and a 2m ID matrix. The last form of the t-symbol matrix parity regulation is the following:

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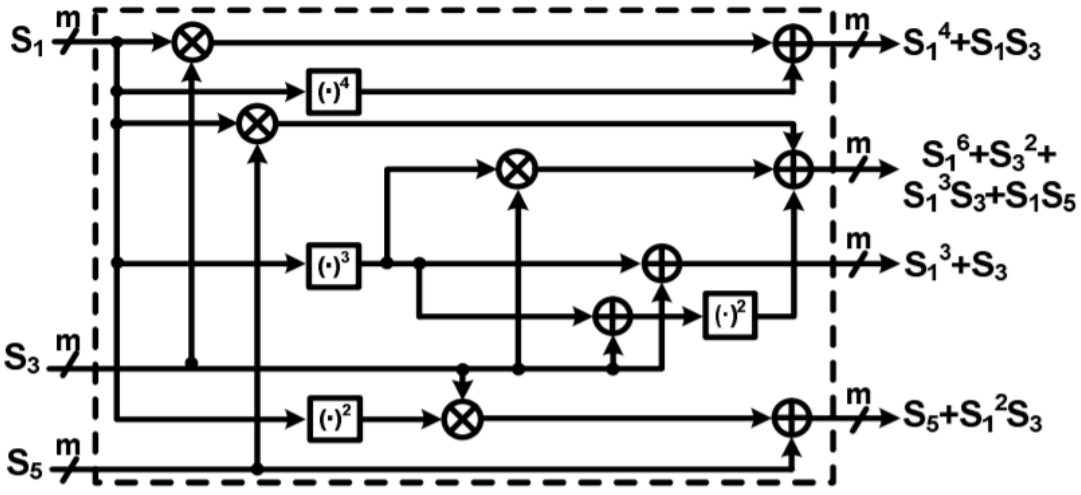
For each Mi Submatrix, a non-zero symbol per column, and a non-zero symbol per column will be available. Non-zero elements are referred to as identity components for the region or GF(2^{10}), which means that for the operations and H is just an additive and a multiplication identity. For hardware, the syndrome generator can only be constructed using q-input XOR gates [29]. It is not necessary to multiply Galois fields as long as there are no different elements than α0. This is critical because of the GF multiplier famine, which means that 64 gates and 48 AD gates equals any GF(2^{10}) multiplier of the Galois fields.

We present a DC architecture parallel to a sharing technique. The proposed DC includes the SSFC as illustrated in fig.3 as well as the Chien Search Block (CS). The SSFs are determined with the values of the syndrome in the SSFC block. The decoding process only requires one clock cycle latency as the SSFs are constant [30]. The BCH multi-channel multi-parallel decoder therefore does not alleviate the SSFC block and can also be exchanged as much as you can with this scheme.

The CS block estimates the value of H with the codeword knowledge using the error location. CS block values A, B, C and R for the SSFC block sharing factors are given. The CS block controls when an error occurs. The GF multipliers tends to have similar inputs and it is then combined with a single block and then with a iterative matched algorithm of the constant GF multipliers can be used for sharing common factors [31]. The parallel CS block hardware complexity can be reduced substantially. This results in greater hardware efficiency and increased parallel factor in the proposed DC block.



(a) syndrome factor calculator

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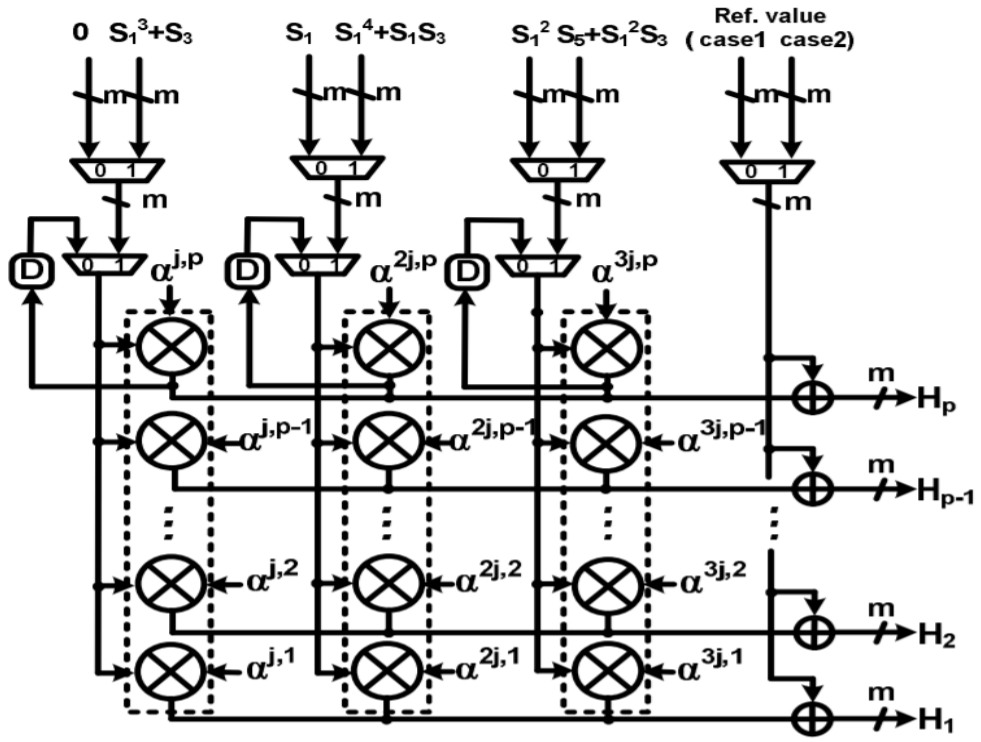

(b) parallel search block

Figure 4. Determinant calculator

***Error Locator*:** EL checks the error location and corrects H-values for errors. The H value is used to changed to a single-bit OR by bit-wise. Two types of values in the proposed method are necessary for checking the error location and fixing errors. In comparison to the H value, the second H-value type checks whether the location of the bit is wrong. This is because the codeword error number is identified through the comparator to observe the first-to-fourth H values. This means that you can gain a reference H value alone. Figure 4 shows the self-error detection.

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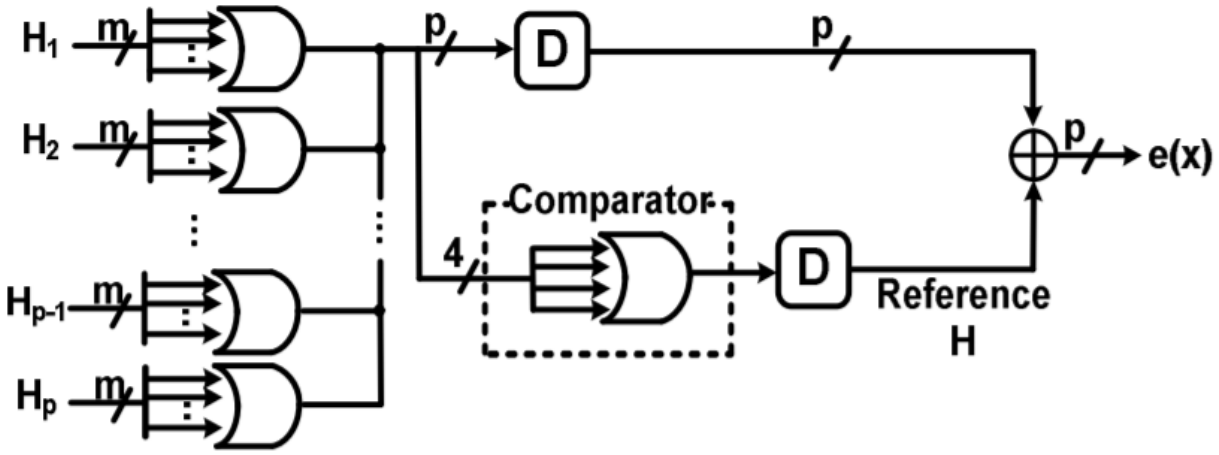

Figure 5. Error locator

***Decoding process*:** In order to calculate the codes of code for decoded code in non-binary parity control codes, a one-step majority logic decoding algorithm [32]. Two main decoding measures are involved: the syndrome calculation; and an extra-information symbol estimate.

RESULTS AND DISCUSSIONS

This section provides the details of evaluation and analysis the proposed low complex decoder design. The study is compared with ECC, Powerful Weight decoder, Kasamis Error trapping decoder, High speed Golay code decoder and Shortened Binary Golay Code. The proposed method is compared with existing methods on various performance metrics that include delay, power dissipation, power savings, and power delay product on various low complex decoder.

Table 1 shows the evaluation of delay over various frequencies. The proposed low complex decoder is compared with existing methods over various input data point. The results shows that the delay is in order of nano seconds. The proposed low complex decoder has reduced delay than the existing methods, where the delay is indirectly proportional to the types of input data points. It is seen that with increasing input data points, the system tends to operate with reduced delay. However, the proposed low complex decoder has lesser delays on all frequencies.

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Table.1 Performance evaluation of delay

Input data points	Delay (ns)					
	High speed Golay code decoder	Kasamis Error trapping decoder	Powerful Weight decoder	ECC	Shortened Binary Golay Code	Low complex decoder
128	10.23	3.08	2.05	2.02	1.73	1.23
256	10.73	3.42	2.31	2.28	1.99	1.32
512	11.25	4.42	3.35	3.31	3.04	3.01
1024	15.63	7.56	6.39	6.32	6.11	5.47

Table 2 shows the evaluation of power dissipation over various frequencies. The proposed Low complex decoder is compared with existing methods over various input data point. The results shows that the dissipation of power is in order of micro watts. The proposed Low complex decoder has reduced power dissipation than the existing methods, where the dissipation of power is indirectly proportional to the input data points. It is seen that with increasing input data points, the system tends to operate with reduced dissipation. However, the proposed low complex decoder has lesser power dissipation on all frequencies.

Table 2. Performance evaluation of power dissipation

Input data points	Power Dissipation (µW)					
	High speed Golay code decoder	Kasamis Error trapping decoder	Powerful Weight decoder	ECC	Shortened Binary Golay Code	Low complex decoder
128	6.53	5.23	4.69	4.59	3.5	3.07
256	11.62	10.54	9.82	9.78	7.07	5.97
512	21.36	19.78	18.54	18.38	12.96	10.75
1024	38.11	36.42	35.53	35.46	24.75	20.32

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Table 3. Performance evaluation of power savings

Input data points	Power Saving (%)					
	High speed Golay code decoder	**Kasamis Error trapping decoder**	**Powerful Weight decoder**	**ECC**	**Shortened Binary Golay Code**	**Low complex decoder**
128	92.1	93.2	94.1	95.4	96.5	96.9
256	85.4	87.6	89	90.2	92.9	94.0
512	73.5	76.5	79.8	81.6	87.0	89.2
1024	58.1	61.4	62.3	64.5	75.2	79.6

Table 3 shows the evaluation of power savings over various frequencies. The proposed Low complex decoder is compared with existing methods over various input data points that includes: N=128, N=256, N=512 and N=1024. The results shows that the power savings is in order of micro watts. The proposed Low complex decoder has higher power savings than the existing methods, where the power savings is indirectly proportional to the input data points. It is seen that with increasing input data points, the system tends to operate with reduced dissipation and hence the power savings is high. However, the proposed Low complex decoder has higher power savings on all frequencies.

CONCLUSION

In this paper, we present the low complex error collection parallel decoding architecture effectively increases the process of decoding. The triple layered mechanism in the low complex decoding architecture reduces the possible errors by locating the error regions without error polynomial computation. Further the utilization of orthogonal Latin squares with Golay codes in Galois field improves the speed with reduced error. The system therefore operates with maximum speed thereby reducing the latency of processing the decoding operations. Evaluation on CMOS 45nm technology shows reducing the latency, capacity, delay and area.

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