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Modified Power Decoupling and Power Processing for Single Phase Led Drive

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Abstract

Reduced power processing is a current trend in LED driver systems in an effort to improve conversion efficiency. This study offers a unique LED driver architecture based on the concept that fewer power semiconductors are required than in earlier work, resulting in the potential for lower costs and greater efficiency. To produce a constant output current and power factor of one with a lot of energy storage, a novel AC/DC LED driver topology has been developed in accordance with the architecture. The 100/120Hz energy buffer has been lowered. Thus, the final structure is identical to that of a standard single-stage PFC, which is indicative of a converter with a high power density. Results in terms of enhanced power quality and conversion efficiency are supported by experimental evaluation.

Keywords— *LED driver, E caps, power decoupling, single phase, power processing*

INTRODUCTION

LEDs are a huge technological development in lighting that can transform how lights work. Its popularity has grown because it works well, lasts long, and is environmentally safe. It is now the main source of artificial light in many situations. They have many advantages over traditional incandescent lighting, but the most important ones are that they last longer, use less energy, and need less maintenance. LED lighting has a huge amount of potential to save energy [1, 2]. An LED Driver is a device that connects a power supply to an LED load and is necessary for optimal functioning. The cost, size, dependability, and light quality of an LED lighting fixture are all factors to consider. Although LED lighting has several advantages, designing an LED driver may be a difficult task [3, 4]. A dedicated LED driver that can transition from alternating current to direct current should supply a controlled DC voltage to power the load while maintaining a high power factor. This is essential for satisfying power demands. In addition to these demands, there has been a rising tendency in recent years toward making AC/DC LED drivers without electrolytic capacitors due to their limited lifespan [5, 6]. E-caps are used to smooth out the twice-line ripple power that is a part of every single-phase system. Active buffering is a good way to deal with the problem we just talked about. In this strategy, ripple power is actively sent to a buffer capacitor. This separates the ripple voltage's strict need from the capacitor's need to store energy, which can be done by increasing the capacitor's voltage swing. Because the amount of energy that needs to be stored is less, the system can use capacitors with a long life without sacrificing power density or cost [7-9]. The design is made up of two stages, first stage handle power factor correction (PFC) and the second stage handles current regulation. The ripple power is absorbed by the buffer capacitor Cdc. Allowing a greater voltage swing on the Cdc can effectively lower its capacitance [10-12].

The main aim of the circuit is to regulate switching current in order to achieve high power factor correction requirements while preserving DC load output current. This is accomplished by using AC as the input source and correcting the AC source to DC. For the conversion procedure, a bridge rectifier MOSFET is employed as a switch. After conversion, a storage device such as a capacitor is utilized, and the supply to the load is maintained.Proposed model of LED Driver architecture is shown in the fig 1.

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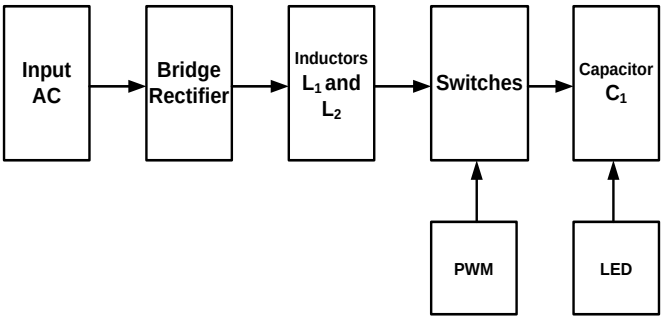

Fig.1 Block diagram of proposed topology

Some of the best related works were taken and their key factors are discussed as follows;

- The design of AC-DC LED drivers should strive to do away with the use of E-caps. This research suggests using an energy-buffering LED driver to do rid of flickering lights altogether. The DC LED output current is maintained via power factor adjustment with a high value. The ideal LED driver would be one that adjusted for current ripple and did not require E-caps. Electrolytic capacitors with a short lifespan. The lifespan of LED driver components is shortened by capacitors [13]. Within the recommended LED driver is a combination of high-voltage film capacitors and a Buck converter to buffer imbalanced energy. An AC–DC LED driver that incorporates a rectifier and an auxiliary circuit is suggested in this article.
- The suggested LED driver uses fewer active power components and less redundant power processing. Half-bridge LLC resonant converters use one inductor and two switches. BCM rectifies both boost circuits' power factor [14].
- A low-power LED off-line driver is constructed by splitting the LED driver's input voltage with two capacitors to lower the bus voltage to the input peak voltage. This effective research makes use of MPP. Almost-perfect PFC is generated via a straightforward dual-output DCM PWM front-end converter [15].
- The zero-low-level square-wave driving current technique reduces LED driver storage capacitance by 53.7% compared to constant dc driving current. During PWM dimming, the capacitor voltage is analysed and validated [16].

PROPOSED SYSTEM

This paper offers a unique AC/DC design for low-power computing. The configuration features a bidirectional PFC as well as a DC/DC stage. Ps and Pd input power losses are eliminated owing to the two outputs. The method reduces expenses, simplifies topology, and improves efficiency. This work shows PFC stage with two outputs using a common inductor, avoiding additional magnetic storage as in earlier implementations. Fig.2 shows the proposed model.

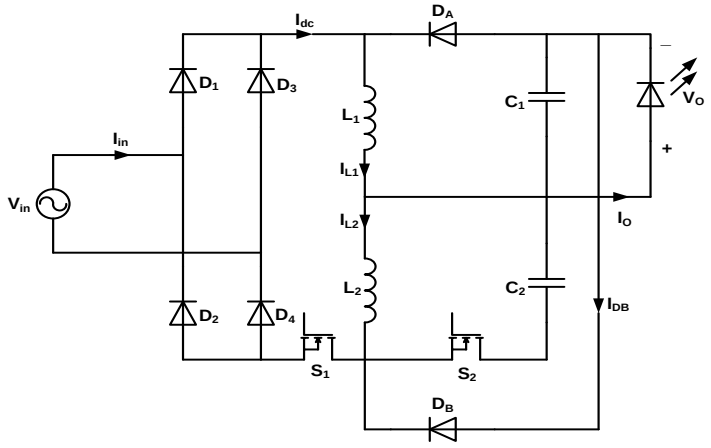

Fig.2. Circuit diagram of modified topology

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Single-stage buck-boost topology is presented in figure 2. This is a two-step process. To serve as a two-output PFC converter, the buck-boost primary inductor is split. An additional power flow channel that is formed by S_2, C_2, and D_B emulates the DC/DC converter for Pc(t) and active buffering by sharing L_2 with the two-output Power Factor Correction (PFC) converter. This channel is responsible for the flow of power.

a. Modes of operation

The suggested architecture operates in discontinuous conduction mode (DCM), which is quite similar to the typical buck-boost converter. This allows for a high power factor to be achieved. There are five modes of operation. The comparable circuit for each mode is presented. The appropriate waveforms are illustrated in figure 3.

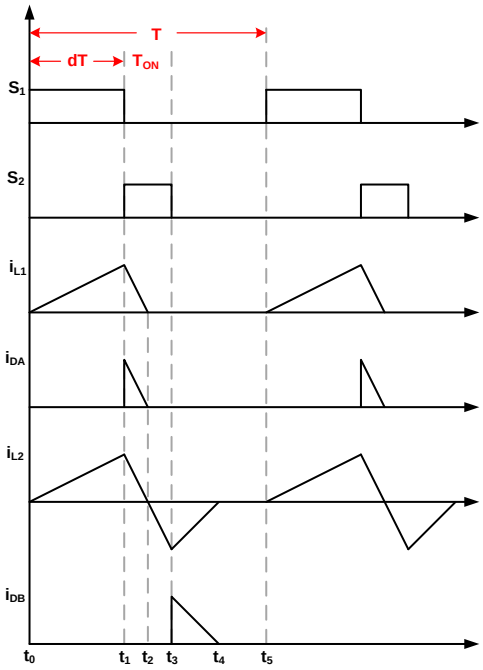

Fig.3. Functioning waveforms

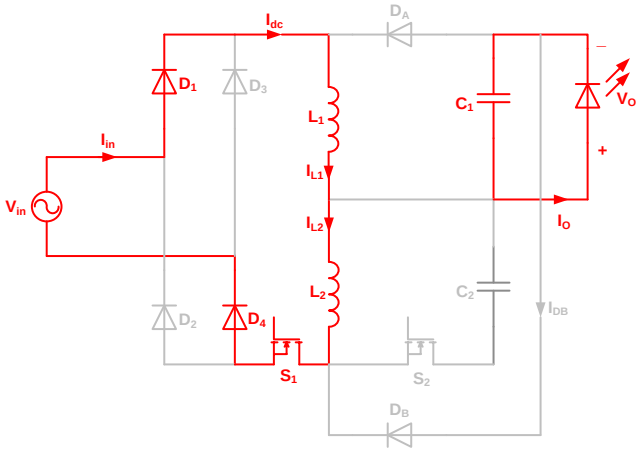

Fig.4(a). Mode 1

during **mode 1,** switch S_1 is triggered on at the initial time period t_0**.** The input voltage concurrently charges both La and Lb until S1 is shut off at t_1, as illustrated in Fig.4(a).

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During this mode, the peak inductor current, $i_P(t)$, may be calculated using (1)

$$i_p(t) = \frac{|Vin(t)|D}{(L_1+L_2)f_s} \quad (1)$$

The duty cycle for S_1 is D, and the switching frequency is fsw. During this mode of operation, input current is same as the current flowing through the inductor and reduced to zero in all other modes, the average input current during this mode is given in (2)

$$i_{avg}(t) = D \times i_p(t) = \frac{D^2|V_{in}(t)|}{(L_1+L_2)f_s} \quad (2)$$

Power factor adjustment occurs naturally at a constant duty ratio because input current is the function and proportional to input voltage.

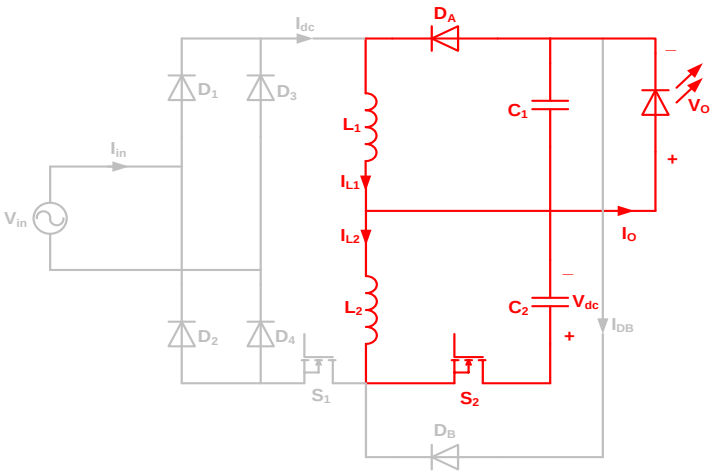

Fig.4 (b). Mode 2

Mode 2 [t_1-t_2]: At time t_1, S_1 is disabled. The energy stored in La is supplied directly to the LEDs via D_A without being processed, producing the primary power flow channel, P_m, as evidenced by the fact that L_1 is completely drained at time t_2.Meanwhile, as shown in Fig. 4(b), the energy held in L_2 is first released to the buffer capacitor through S_2, resulting in the reprocessed power, $P_r(t)$, When $i_{L2}(t)$ reaches 0, the buffer capacitor reverses the charge on L_2, making i_{L2} negative. S_2 is given a short dead-time to guarantee that its output capacitance is fully depleted before it can be switched on. When L_2 releases power, S_2 acts as a synchronous rectifier, lessening conduction loss.

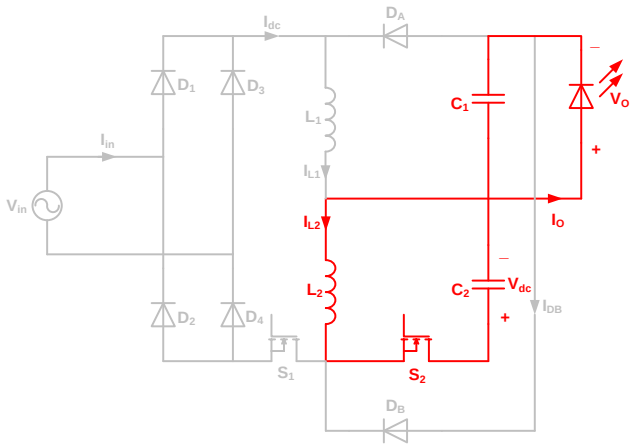

Fig.4(c). Mode 3

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Mode 3 [t_2-t_3]: In the same manner as a conventional buck-boost converter, the capacitor C_2 charges L_2. $T_{on}(t)$, the on-time of S_2, as depicted in fig 4(c) influences the amount of energy released from the capacitor C_2 to generate $P_c(t)$ and is utilized as a control variable to ensure a constant output current.

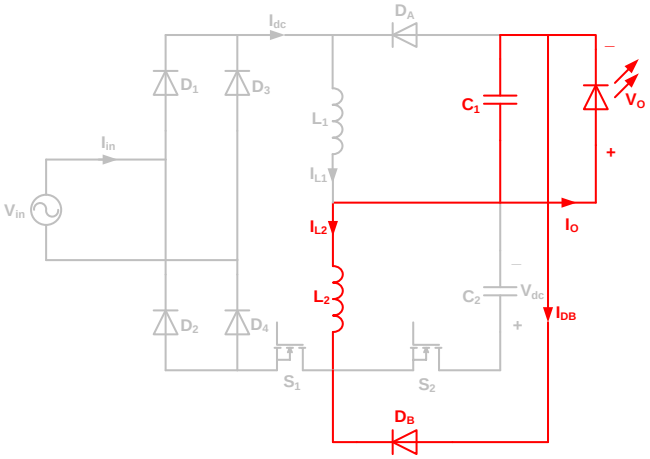

Fig.4(d). Mode 4

Mode 4 [t_3-t_4]: At t_3, S_2 is turned off, as shown in Fig.4(d), and the energy stored in the inductor L_2 is transmitted to the load LED via D_B, resulting in $P_c(t)$. L_2 is completely released at t_4.

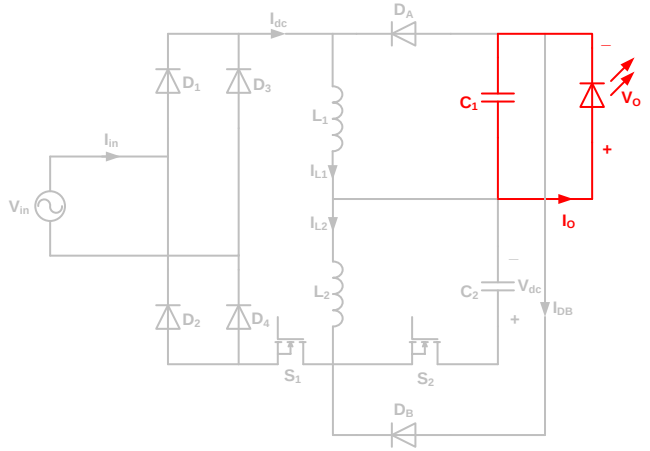

Fig.4(e). Mode 5

Mode 5 [t_4-t_5]: During this mode, energy stored in both inductors is discharged, and the load power is maintained by the output capacitor, as represented in figure 4(e).

b. Design of Inductors

Furthermore, the k ratio must be selected so there is sufficient energy to produce the required power and negate the ripples in $P_m(t)$. The k value should be at least 0.5 for the goal to be met. So that power losses during the stage of reprocessing can be taken into account, k should be a little more than 0.5.Assuming that the DC to DC conversion stage is efficient, the k should be selected so that

$$\eta AVG(P_r(t)) > AVG(P_m(t)) \quad (3)$$

The average operator across a line time is the AVG (). We can get

$$k > \frac{1}{1+\eta} \quad (4)$$

After solving, (L_1 + L_2) should be built in such a way that the converter continues to work in discontinuous conduction mode. Every switching period, the inductors should be fully drained to sustain DCM functioning. As demonstrated, the conduction time of Lb may be separated into four sections: $T_{on.a}(t)$, $T_{off.a}(t)$, $T_{on.b}(t)$, $T_{off.b}(t)$ can be calculated using (5)-(8)

$$T_{on,a}(t) = \frac{\sqrt{4(L1+L2)Ts\ Po}}{Vin} \quad (5)$$

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$$T_{off.a}(t) = \frac{k|\sin(\omega t)|\sqrt{4(L1+L2)Ts\ Po}}{Vdc(t)} \quad (6)$$

$$T_{on.b}(t) = \frac{\sqrt{4(1-k)L2\ Ts\ Po\ \cos 2(\omega t)+2(2k-1)L2\ Ts\ Po}}{Vdc(t)} \quad (7)$$

$$T_{off.b}(t) = \frac{\sqrt{4(1-k)L2\ Ts\ Po\ \cos 2(\omega t)+2(2k-1)L2\ ts\ Po}}{Vo(t)} \quad (8)$$

Solving the following inequality yields the highest value of (L_1 + L_2) that permits the converter to function in DCM:

$\max(T_{1,on}(t) + T_{1,off}(t) + T_{2,on}(t) + T_{2,off}(t)) \leq T_s$.

Taking into account grid voltage fluctuations and load variations, there should be a safety buffer, and the (L_1+L_2) should be set somewhat lower than its higher value.

RESULTS AND DISCUSSION

The modified topology has been designed in simulation and tested using a hardware prototype to verify the characteristics and working. Results of hardware prototype and simulation are presented and analysed in this section. The converter circuit was simulated using MATLAB/Simulink R2019b environment. Input of 230V was given to the circuit and the waveform is depicted in figure 5.

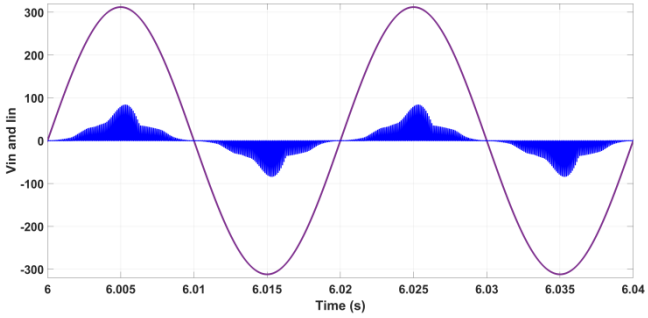

Fig.5. Input Voltage and Current

The output voltage measured across the load shown in figure 6. It is observed that the output is maintained almost constant value as the oscillations are minimum.

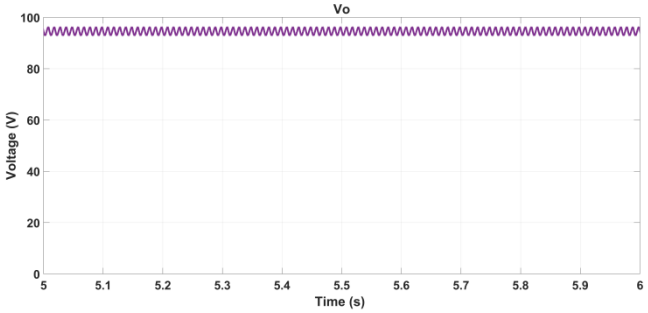

Fig.6. Output voltage waveform

The voltage waveform across the capacitor C_1 is produced in figure 7. Based on the charging and discharging times and voltage value of the capacitor, it is observed that the voltage-second balance of capacitor C_1 is zero, which is acceptable.

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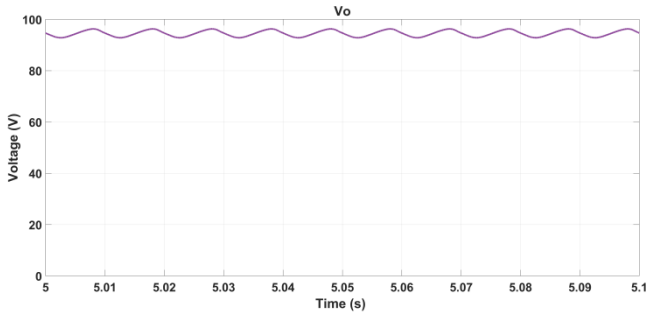

Fig.7. voltage waveform across C_1

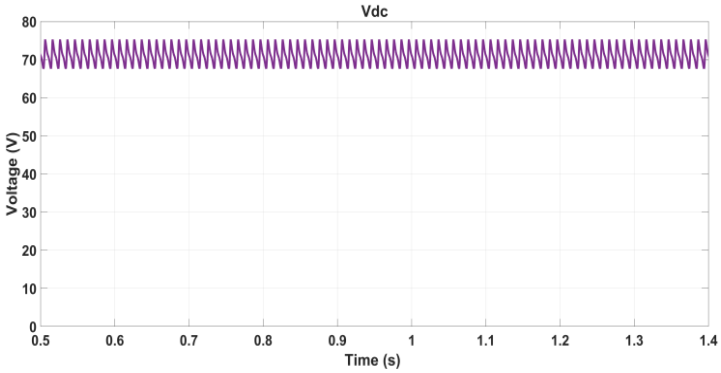

Fig.8. Voltage across capacitor C_2

The corresponding DC voltage across the buffer capacitor is constant with slightly higher time constant value. Voltage across the buffer capacitor shown in figure 8 is constant and higher than the output voltage. The voltage waveform across the buffer capacitor C_2 is produced in figure 9. Based on the charging and discharging times and voltage value of the capacitor, it is observed that the voltage-second balance of capacitor C_2 is close to zero, which is acceptable.

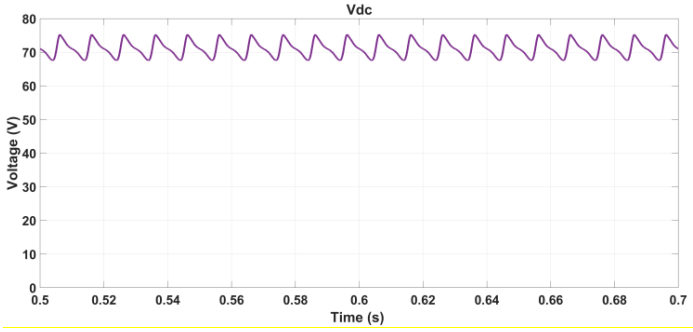

Fig.9. Charging and discharging of C_2

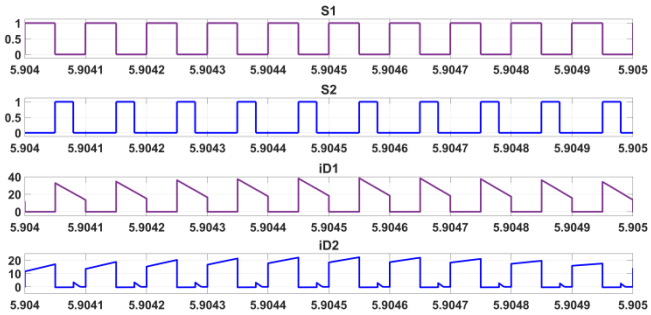

Fig.10. Diode currents with switching pulses

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Fig.11. Inductor currents with switching pulses

Inductors L_1 and L_2 are charging and discharging at discontinuous mode, as discussed in previous sections. Inductor L_1 charges in forward direction and L_2 charges in reverse direction. On and Off time of switches are described using the charging and discharging time of the inductor L_2.

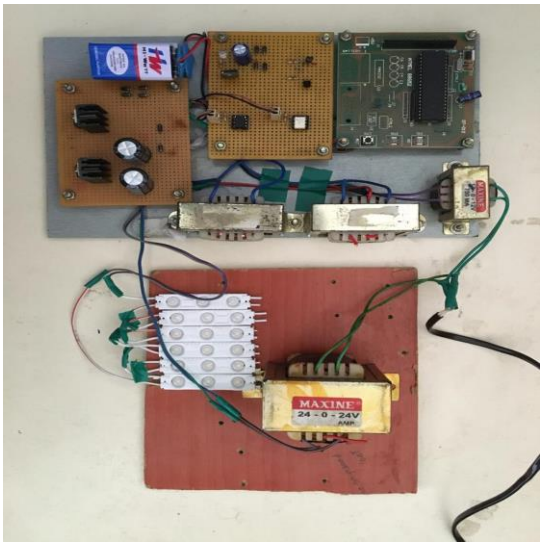

Fig.12. Hardware prototype

Inductor L_2 discharges before the next switching cycle as mentioned earlier. Diodes D_A and D_2 carry current during the switching interval as shown in figure 10 and the corresponding inductor currents are mentioned in figure 11.

Simple and effective, automated power decoupling is chosen. D controls input power. Input and output power must be balanced and VDC must be constant during each line period. As a result, D governs VDC. The PWM signal for S_1 is created by comparing the dc voltage to the saw tooth signal. Ton (t) controls output current. A 10W model was developed to evaluate the functionality of the suggested topology as shown in figure 12. The design specifications of the prototype are shown in Table 2. Thus, it is possible to obtain sinusoidal input current and a persistent output current.

TABLE.1 27W PROTOTYPE KEY PARAMETERS

Parameters	Values
Input voltage, Vin	230V, AC (RMS)
Power	40W
Line frequency	50Hz
C_1	3.3mF
C_2	20mF
L_a	200µH
L_b	250µH
Diodes (D_a and D_b)	1N4007

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Switches (S1 and S2)	IRF840
Output voltage	96V
Switching frequency	10kHz

Figure 13 shows the output voltage and capacitor voltage waveforms. It is observed that the output voltage is maintained as constant value of 96 V and the corresponding value of buffer capacitor voltage is 60V.

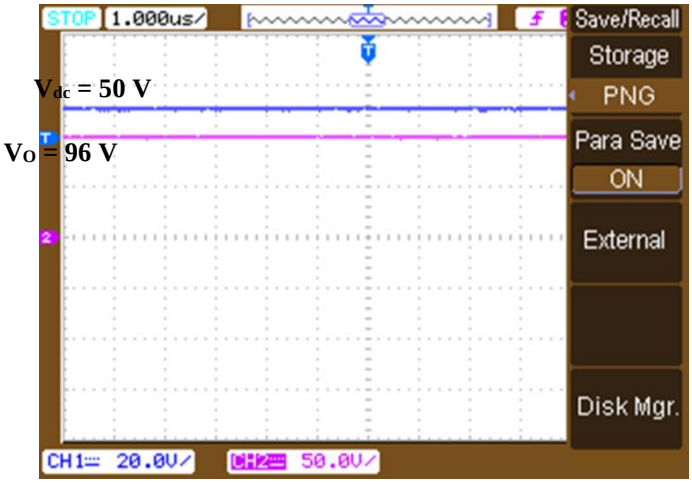

Fig.13. Output voltage and capacitor voltage waveforms

CONCLUSION

This research presents a ground-breaking LED driver that, in comparison to previously published architectures, has a lower power consumption, fewer switches, and smaller magnetics. In contrast to the more traditional single-stage approaches, the suggested design is able to successfully provide active buffering and reduce the amount of power processing by making use of a divided and shared inductor. The proposed driver has been shown to obtain a high value of power factor, maximum efficiency, and a steady output current, as demonstrated by the results of several experiments. In addition to this, it illustrates the usefulness of analogue control circuits that can be fully incorporated at some point in the future. The proposed design not only makes the driver circuit more straightforward, but it also does away with the need for electrolytic capacitors, which are known to have an exceptionally long lifespan.

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